IN THE CLAIMS

For the convenience of the Examiner, all pending claims of the present Application are presented below whether or not an amendment has been made. Please amend the claims as follows:

1. **(Currently Amended)** A method for error detection in a high-speed switching environment, comprising:

receiving, at a switch input port, a plurality of packets, including a first packet having at least first and second portions;

initiating switching of the first portion before the entire second portion is received at the switch input port; ~~and~~

using tag data associated with the first packet to calculate error detection data for the first packet, the error detection data calculated **at the switch** before the entire second portion is received at the switch input port;

at the switch, inserting the error detection data calculated using the tag data into the plurality of packets; and

performing an error detection technique on the first packet using the error detection data that was calculated using the tag data associated with the first packet.

2. **(Original)** The method of Claim 1, wherein the initiating switching of the first portion is accomplished in accordance with a cut-through forwarding technique.

3. **(Original)** The method of Claim 1, wherein the initiating switching of the first portion is accomplished in accordance with a delayed cut-through forwarding technique.

4. **(Original)** The method of Claim 1, further comprising looking up a tag ID for association with the first packet.

5. **(Original)** The method of Claim 4, further comprising assigning the tag ID to the first packet.

6. **(Original)** The method of Claim 1, further comprising receiving the first portion at the switch output port, wherein the error detection is performed at the switch output port.

7. **(Original)** The method of Claim 1, wherein the error detection technique is accomplished according to a limited cyclical redundancy checksum technique.

8. **(Currently Amended)** The method of Claim 7, wherein the cyclical redundancy checksum technique includes recalculating a CRC of the first packet based only upon changes in the ~~**tag ID**~~ **tag data** of the first packet.

9. **(Currently Amended)** A system for error detection in a high-speed switching environment, comprising:

a first switch input port being operable to receive a plurality of packets, the plurality of packets including a first packet having first and second portions;

a switch core operable:

use tag data associated with the first packet to calculate error detection data for the first packet, the error detection data calculated **by the switch core** before the entire second portion is received at the switch input port; ~~**and**~~

insert the error detection data calculated using the tag data into the plurality of packets; and

switch the first portion before the entire second portion is received at the first switch input port; and

a detection module being operable to perform an error detection technique on the first packet using the error detection data that was calculated using the tag data associated with the first packet.

10. **(Original)** The system of Claim 9, wherein the first switch input port is further operable to lookup a tag ID for association with the first packet.

11. **(Original)** The system of Claim 10, wherein the first switch input port is further operable to assign the tag ID to the first packet.

12. **(Original)** The system of Claim 9, further comprising a switch output port being operable to receive the first portion of the first packet.

13. **(Original)** The system of Claim 12, wherein the switch ouput port comprises the error detection module.

14. **(Original)** The system of Claim 13, wherein the error detection technique is accomplished according to a limited cyclical redundancy checksum technique.

15. **(Currently Amended)** The system of Claim 14, wherein the cyclical redundancy checksum technique includes recalculating a CRC of the first packet based only upon changes in the ~~**tag ID**~~ **tag data** of the first packet.

16. **(Original)** The system of Claim 15, wherein the first portion is switched in accordance with a cut-through forwarding technique.

17. **(Original)** The system of Claim 15, wherein the first portion is switched in accordance with a delayed cut-through forwarding technique.

18. **(Currently Amended)** A system for performing error detection in a high-speed switching environment, the system comprising:

one or more memory structures;

a plurality of input structures that are each operable to receive a packet communicated from a component of a communications network and write the received packet to one or more of the one or more memory structures;

a first switching structure coupling the plurality of input structures to the one or more memory structures such that each of the plurality of input structures are operable to write to each of the one or more memory structures;

a plurality of output structures that are each operable to read a packet from one or more of the one or more memory structures for communication to a component of the communications network;

a second switching structure coupling the plurality of output structures to the one or more memory structures such that each of the plurality of output structures are operable to read from each of the one or more memory structures, an output structure being operable to read a first portion of one of the packets from one or more of the one or more memory units for communication to a first component of the communications network before an input structure has received a second portion of the one of the packets communicated from a second component of the communications network; and

a detection module being operable to perform an error detection technique on the packet using error detection data inserted into the first portion of the packet before an associated second portion of the packet is received by the plurality of input structures, the error detection data calculated **at the switch** using tag data associated with the packet **and inserted into the packet at the switch**.

19. **(Original)** The system of Claim 18, wherein the memory structures are operable to store tag IDs for association with the packets.

20. **(Original)** The system of Claim 19, wherein the error detection technique is accomplished according to a limited cyclical redundancy checksum technique.